Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GEORGE M. BRACERAS
and LAWRENCE C. HOWELL, JR.

Appeal No. 2002-0374
Application No. 08/599,227

ON BRIEF

Before HAIRSTON, BARRY, and LEVY, Administrative Patent Judges.

LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-13[1], which are all of the claims pending in this application.

BACKGROUND

Appellants' invention relates to a system and method for accessing a cache memory having a redundant array without displacing a cache line in a main memory. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced as follows:

1. An improved cache memory system, comprising:

a plurality of cache lines in a cache;

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[1] An amendment (Paper No. 18, filed January 27, 1997) submitted subsequent to the final rejection (Paper No. 17, mailed November 25, 1996) was not initially entered by the examiner (Paper No. 19, mailed February 12, 1997). However, the examiner indicated that the rejection of claims 1 and 2 under 35 U.S.C. § 112, second paragraph, was withdrawn in view of appellants' response. In a supplemental advisory action (Paper No. 20, mailed March 11, 1997) the examiner indicated in box 1 that the amendment would not be entered for purposes of appeal. However, in box 3, the examiner indicated that the amendment would be entered for purposes of appeal. Appellants indicate (brief, page 2) that the amendment was entered by the examiner. The examiner (answer, page 1) confirms that appellants' statement of the amendments after final rejection contained in the brief is correct. Accordingly, we consider the amendment received January 29, 1997 to have been entered. Although the amendment has not been physically entered into the file, we consider this to be a formal matter to be addressed by the examiner subsequent to the appeal. In addition, we observe that the language of claim 1 as amended (Paper No. 18, filed January 27, 1997) is inconsitent with the language of the claim as it appeared in the application prior to the January 27, 1997. In the decision, we have relied upon the language of claim 1 as it appears in the appendix to the brief and in the after final amendment (Paper No. 18, filed January 27, 1997). The examiner should review the amendment and the previous amendment (Paper No. 16, filed September 30, 1996 to determine the actual language of claim 1. As the difference in the language of the claim would not change our decision, infra, we consider this a formal matter to be addressed by the examiner subsequent to the appeal.

at least one redundant unmapped cache line in said cache; and

means for signaling said cache to access one of said plurality of cache lines or said at least one redundant unmapped cache line, wherein said at least one redundant unmapped cache line is used as a temporary cache location without displacing or overwriting any of said plurality of cache lines.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

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| Supnik | 5,070,502 | Dec. 3, 1991 |
| Rastegar | 5,297,094 | Mar. 22, 1994 |

Lucente, "Memory System Reliability Improvement Through Associative Cache Redundancy", Vol. 26, No. 3, March 1991, pages 404-409.

Claims 1-13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Supnik in view of Rastegar or Lucente. Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejection, we make reference to the examiner's answer (Paper No. 24, mailed September 16, 1997) for the examiner's complete reasoning in support of the rejection, and to appellants' brief (Paper No. 23, filed June 6, 1997) for appellants' arguments thereagainst. Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered. See 37 CFR 1.192(a).

## OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejection advanced by the examiner, and the evidence of obviousness relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

Upon consideration of the record before us, we reverse, essentially for the reasons set forth by appellants.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley

Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

We consider first the rejection of claim 1 based on the teachings of Supnik in view of Lucente or Rastegar, each taken separately. The examiner's position (answer, pages 5 and 6) is that "Supnik does not particularly teach a redundant unmapped cache line in the cache, and means for addressing said redundant unmapped cache lines in which said redundant unmapped cache line is used as a temporary cache location without displacing or overwriting any of said plurality of cache lines." To overcome the deficiencies of

Supnik, the examiner turns to each of Lucente or Rastegar. The examiner asserts (answer, page 6) that "Rastegar teaches that it is known to provide a redundant rows [sic] for any particular memory device in which they can be programmed to substitute for array rows containing non-functional bits or defective [bits]." The examiner further asserts (id.) that "Rastegar further teaches . . . [that] the redundant memory is capable of being mapped to any location on the device which contains non-functional memory cells, and incorporating it into the device [of Supnik] should not add complexity to the overall device design." With regard to Lucente, the examiner's position is that Lucente teaches that a cache memory could be modified to provide memory-word redundancy, thereby increasing system reliability as well as throughput. The examiner maintains (id.) that it would have been obvious to include redundant cache lines as they can be substituted for the cache arrays or cache lines which contain non-functional or defective data.

Appellants (brief, page 4) does not dispute that it is well known in the prior art that redundant rows or columns may be substituted for defective rows or columns. Appellants assert (id.) that a premise upon which the invention is based on redundant columns or rows exists and that frequently, not all of the

redundant rows or columns are utilized as defective row or column replacements. Appellants argue that claim 1 recites the provision of a plurality of cache lines and "at least one redundant unmapped cache line in said cache . . . ."

Appellants note (brief, page 5) that in Supnik, a single bit within a cache line is used to indicate whether a fault exists within that cache line. The set reserve bit inhibits the use of a cache line which includes a defect. It is argued that Supnik fails to show or suggest the provision of redundant cache lines, and that nothing within Supnik shows or suggests the provision of unmapped redundant cache lines as set forth in claim 1. Turning to Lucente and Rastegar, appellants assert (id.) that each of these systems disclose the well known technique of providing redundant cache lines which are mapped to a logical equivalent of a defective line. Specifically, Lucente discloses that locations from an on-chip fully associative cache are then mapped into the address space in place of faulty locations, and (brief, page 6) Rastegar discloses that "the columns containing bad links are disabled, typically by blowing fuse links, and the redundant columns are enabled to take their place. Mapping must be done in order to allow the redundant memory to substitute for bad regions anywhere on the device." Appellants urge (brief, page 6) that "[a]pplicant respectfully

urges that nothing within the cited references within the present record shows or suggests in any way the utilization of a 'redundant unmapped cache line' as a temporary cache location as each of the references cited by the Examiner which teaches the utilization of redundant cache lines expressly teaches that those cache lines must be 'mapped' into the cache in order to be utilized."

From our review of Supnik, we find that data errors may be caused, inter alia, by hardware faults, such as defective memory storage cells (col. 7, lines 12 and 13). Densely packed storage cells of high speed cache memories are susceptible to hardware defects. In order to use cache memories which include a few defects, an additional bit 58, 60 called a "defect bit" is incorporated into each entry in the tag storage portions 42, 44 of cache 22. If the defect bit is set, then the entry contains a defect and will no longer be used (col. 7, lines 12-22). Once set, the defect bit essentially removes the entry from the cache (col. 7, lines 31 and 32). The error detecting program (figure 3) loads all of the memory locations with zeros and then with ones. If any bit in the memory locations cannot become a binary zero and a binary one, then the error bit in that location is set so that the memory location is disabled (col. 7, lines 43-54). Thus, we find from our review of Supnik that Supnik disables defective bits by

setting a defect bit to prevent further use of the memory location.

Turning to Lucente (page 404) we find that Lucente discloses that "[t]his device isolates hard errors in system memory by writing a true and complement[ary] pattern to each system memory location. Locations from an on-chip associative cache are then mapped into the address space in place of the faulty locations." When a faulty system memory location is located during system testing, its address is placed in the address tag of one cache location. The location of the failed bit or bits is also stored. All accesses calling for the faulty location will now be directed to the replacement cache location the architecture of Lucente (page 408) is implemented in a Memory Reliability Enhancement Peripheral (MREP) device. The MREP provides redundancy at a system level by using its on-chip cache to replace failed words anywhere in the memory system. In addition (id.) "[a]s each failed memory location is detected, a cache location replaces it." Thus, from the disclosure of Lucente, we find that Lucente replaces defective bits by replacing them with a location in cache, and does not disclose the provision of unmapped cache locations which can be used as temporary cache without displacing or overwriting portions of the memory.

Turning to Rastegar, we find that a processor, when accessing a memory, accesses the desired memory location through the cache. If the memory location is not in the cache, the memory location is fetched from the main memory (col. 1, lines 35-39). It is known that memory devices have non-functioning bits as a result of processing variations. Rather than discard devices having a small number of ad bits, redundant memory cells are provided. The columns containing bad bits are disabled, typically by blowing fuse links, and the redundant columns take their place. Mapping must be done to allow the redundant memory to substitute for bad regions anywhere on the device (col. 2, lines 9-19). In Rastegar, redundant rows are provided to substitute for array rows containing non-functional bits (col. 2, lines 40-42). The memory array is divided approximately in half. The bit lines cross over between array halves to minimize stray capacitance and cross-coupling capacitance. The redundant rows can be located in the first half of the array. The second half of the array provides inverted data. If a redundant row replaces an array row in the second half of the array, the data must be inverted prior to writing to or reading it from the redundant row (col. 2, lines 35-51). Rastegar further discloses (page 9, lines 25-30) that "[i]t is well known in the art that redundant memory cells can be provided for memory arrays in

order to replace bad memory cells. Enough spare rows or columns must be provided to replace all of the rows containing bad bits in most cases, but it is undesirable to provide too many redundant rows."

From the disclosure of Rastegar, we find that Rastegar discloses replacing defective rows with redundant rows in the cache, and mapping the replacement rows to the location of the defective rows. We find no teaching or suggestion in Rastegar of accessing unmapped cache lines as temporary cache locations without replacing or overwriting any contents within the main memory array, as required by claim 1. Thus, we find that the prior art references to Lucente and Rastegar would have suggested replacing defective lines in Supnik with redundant cache lines, but do not teach or suggest accessing redundant unmapped cache lines, and using the unmapped redundant cache lines a temporary cache without displacing or overwriting any contents within the main array.

We are not persuaded by the examiner's assertion (answer, page 10) to the effect that Rastegar's teaching of mapping redundant memory to any location on the device which contains non-functional data, suggests that when being used as a temporary cache location, mapping is necessary, and redundant unmapped cache lines are used. We find the examiner's assertion to be unsupported by any evidence

in the record, and to be the result of using appellants' invention as a template, in a hindsight reconstruction of appellants' invention. We note again the statement in Rastegar (col. 9, lines 25-30) that enough spare rows or columns should be provided to replace all of the rows containing bad bits, but that it is undesirable to provide too many redundant rows. If Rastegar disclosed the use of redundant rows as redundant unmapped cache locations, Rastegar would have been motivated to provide as many redundant rows as possible to increase the useable size of the cache memory. We find no teaching or suggestion in Rastegar, and no portion of Rastegar has been pointed to by the examiner, which would suggest using the redundant memory as temporary cache locations, resulting in the utilization of the redundant memory as redundant unmapped cache lines.

We agree with the examiner that the redundant memory of Rastegar could be used as redundant unmapped cache lines, but find no teaching or motivation to have done so. Similarly, with respect to Lucente, because Lucente discloses replacing failed memory locations with memory from the cache, we find no suggestion of using the cache memory as redundant unmapped cache lines which are used as temporary cache without displacing or overwriting any of the lines of memory. From all of the above, we find that the

examiner has failed to establish a prima facie case of obviousness of claim 1. Accordingly, the rejection of claim 1 under 35 U.S.C. § 103(a) is reversed. As the other independent claims require either redundant unmapped cache lines and/or accessing the redundant cache line without displacing the data in the main array, we find that the teachings of Supnik, Rastegar and Lucente do not suggest the language of claims 2-13. In sum, the rejection of claims 1-13 under 35 U.S.C. § 103(a) is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-13 under 35 U.S.C. § 103 is reversed.

REVERSED

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| KENNETH W. HAIRSTON<br>Administrative Patent Judge | ) |
| LANCE LEONARD BARRY<br>Administrative Patent Judge | ) BOARD OF PATENT APPEALS AND INTERFERENCES |
| STUART S. LEVY<br>Administrative Patent Judge | ) |

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BRACEWELL & PATTERSON, L.L.P.
INTELLECTUAL PROPERTY LAW
P. O. BOX 969
AUSTIN, TX 78767-0969